SESSION 9 – TAPA I
Multi-Channel Transceivers

Friday, June 18, 10:20 a.m.
Chairpersons: W. Lee, Texas Instruments
H. Ikeda, Elpida

9.1 — 10:20 a.m.
5-6.4Gbps 12 Channel Transceiver with Pre-Emphasis and Equalizer, H. Higashi, S. Masaki, M. Kibune, S. Matsubara, T. Chiba, Y. Doi, H. Yamaguchi, H. Takauchi, H. Ishida, K. Gotoh and H. Tamura, Fujitsu, Ltd., Kawasaki, Japan

A 5-6.4 Gbps parallel 12-channel IO with a transmitter pre-emphasis filter and receiver equalizer was implemented in 0.11 µm CMOS. The pre-emphasis transmitter that composed of cascade current mirrors can compensate for loss upto 20 dB. The equalizer has an equal path delay among pre-filters, thus can compensate loss up to 15 dB. Moreover we have implemented ISI monitor that enables not only an adaptive equalization but also equalizer-offset cancellation. The transceiver's measured results meet the OIF CEI specification.

9.2 — 10:45 a.m.
A 1-4 Gbps Quad Transceiver Cell Using PLL with Gate Current Leakage Compensator in 90nm CMOS, Y. Frans, N. Nguyen, B. Daly, Y. Wang, D. Kim, T. Bystrom, D. Olarte and K. Donnelly, Rambus, Inc., Los Altos, CA

A quad transceiver cell is designed and implemented in 90nm CMOS technology with a 1V nominal supply. To minimize area and power consumption, the cell uses a single dual-loop PLL. Gate-current leakage compensator is used to mitigate gate-current leakage in the PLL loop-filter capacitor. The quad cell consumes 73mW/link at 3.125 Gbps with 500mV output swing driving double-terminated links and achieves a peak-to-peak transmit jitter of 42ps at 4Gbps data rate.

9.3 — 11:10 a.m.
A 4-Channel 3.125Gb/s/ch CMOS Transceiver with 30dB Equalization, W. Gai, Y. Hidaka, Y. Koyanagi, J.H. Jiang, H. Osone and T. Horie, Fujitsu Laboratories of America, Inc., Sunnyvale, CA

A 4-channel 3.125Gb/s/ch CMOS transceiver has been developed. The receiver includes a second-order derivative analog equalizer to compensate the frequency-dependent attenuation. Equalization can be performed adaptively through monitoring the residual inter-symbol-interference. To talk with a system without receiver equalization, a multiple-tap filter for pre-emphasis is implemented in transmitter. Either pre-emphasis or analog filter is capable of 30dB equalization. Evaluation shows lower than 10-12 BER has been achieved with 30-meter AWG 24 cable.

9.4 — 11:35 a.m.
Power Analysis for High-Speed I/O Transmitters, H. Hatamkhani and C.-K.K. Yang, University of California, Los Angeles, CA

This paper studies the design tradeoffs to minimize power dissipation of multi-Gbps parallel I/O transmitters. A macromodel of a transmitter that can be optimized for power is presented. Also discussed is a means to consider the impact of deterministic jitter due to on-chip buffering on power dissipation. The model allows analysis that considers varying design constraints, and circuit architectures. It provides guidelines on the choice of architecture, and data-rate to achieve large aggregate I/O bandwidths.

Lunch 12:00 pm